ABSTRACT

We have presented here magnetic tunnel junction (MTJ) model based universal NAND and NOR logic gates and studied the proposed universal gates by both experimental and simulation methods. Experimental results substantiates with both the simulated and theoretical results.

INTRODUCTION

Magnetic Tunnel Junction (MTJ) device is presently a very promising device because of its mesmerizing physics, their non-volatility, reconfigurable capability, fast-switching speed, small-dimension, CMOS compatibility, and also its different applications areas like spintronics logic devices and circuits, magnetic storage devices, magnetic sensors and communication etc. Recently, researchers have been established the MTJ based different logic gates [1-6] and in these developed logic gates, MTJs have used as main devices for logical computations and intrinsically enable logic-in-memory architectures with no need for extra hardware. In a logic mode the MTJs act as the basic elements for computations and in a memory mode they are used for non-volatile storage purposes. This enables for the expanding of non-volatile electronics from memory to logical computing applications without any sensing amplifiers and intermediate circuitry as compared to the hybrid CMOS based non-volatile logic circuits. MTJ is a spintronic device which gives a spin orientation in two opposite direction - one parallel and another anti-parallel (shown in Fig.1) i.e. MTJ behaves as a resistor with two resistance characteristics (high and low) depending on the direction of magnetization in the two ferromagnetic layers. Electrically this resembles with diode behavior with high current in the forward direction and low current in the reverse direction.

Here we have exploited the above-mentioned properties to realize the universal NAND and NOR logic gates [7] with a simple behavioral model of MTJ device (shown in Fig. 2) which has been represented as two identical diodes with a low resistance ($R_P$) during parallel magnetization and high resistance ($R_{AP}$) during anti-parallel magnetization.

![Fig.1: MTJ with high and low resistance state](image)
THEORY

The proposed MTJ model based NAND and NOR gates have been shown in Fig. 3a and Fig. 3b, respectively. For both the bidirectional current sources (I\(_1\) and I\(_2\)), we have developed two opamp (OP07) based voltage to current converter (VIC) [8] with MTJ model as grounded load which is shown in Fig. 4. When the input currents are positive values, the currents (I\(_1\) & I\(_2\)) (flow directions have shown with black colored arrow) flow in the path containing R\(_L\), R\(_P\) and diode D\(_1\). The resistances R\(_P\) resemble the low resistance during the parallel magnetization for both MTJs. When the input currents are negative values, the currents (I\(_1\) & I\(_2\)) (flow directions have shown with pink colored arrow) flow in the path containing R\(_L\), R\(_{AP}\) and diode D\(_2\). The resistances R\(_{AP}\) resemble the high resistance during the anti-parallel magnetization for both MTJs.

For VIC with grounded load (Fig.4), the currents (I\(_1\) & I\(_2\)) can be expressed as

\[
I_1 = \frac{V_1}{R} \quad (1) \quad \text{and} \quad I_2 = \frac{V_2}{R} \quad (2)
\]

The currents I\(_1\) and I\(_2\) will be either positive or negative depending on the polarity of voltages V\(_1\) and V\(_2\).
b) The operation of NAND logic gate (Fig. 3a) is explained as follows: when the input currents \( I_1 = -1.021 \text{mA} \) (logic '0') and \( I_2 = -1.021 \text{mA} \) (logic '0'), the output voltage can be written as

\[ V_0(00) = V_{ref} - (I_1 - I_2)R_L \]

where \( V_0(00) \) is the circuit output voltage when \( I_1 = -1.021 \text{mA} \) (logic '0'), \( I_2 = -1.021 \text{mA} \) (logic '0') and \( V_{ref} = +1.000 \text{V} \), the reference voltage.

Similarly, the output voltages are:

\[ V_0(01) = V_{ref} - (I_1 + I_2)R_L \]

when \( I_1 = -1.021 \text{mA} \) (logic '0'), \( I_2 = +1.021 \text{mA} \) (logic '1')

\[ V_0(10) = V_{ref} - (I_1 - I_2)R_L \]

when \( I_1 = +1.021 \text{mA} \) (logic '1'), \( I_2 = -1.021 \text{mA} \) (logic '0')

\[ V_0(11) = V_{ref} - (I_1 + I_2)R_L \]

The operation of NOR logic gate (Fig. 3b) is same as the operation of NAND logic gate (Fig. 3a) even the equations (Eqn.3 to Eqn.6) are also same except the value of \( V_{ref} \) which is -1.000V.

Since we have taken the diode pairs from the transistor array of IC LM389 (Make: Texas Instrument) [9], we have considered here the diodes are identical in all respects i.e. \( V_{D1} = V_{D2} = V_D \)

Equation (3) to equation (6) signify that when input voltages are positive, the forward currents follow the the low resistance (\( R_P \)) paths and when input voltages are negative, the reverse currents follow the the high resistance (\( R_{AP} \)) paths. It is very obvious that the above output voltage equations are independent of diode voltage (\( V_D \)) and hence these parameters are independent of ambient temperature effect also as diode voltage varies with ambient temperature.
RESULTS AND DISCUSSIONS

We have exploited the circuit of Fig.3 for both simulation study using sophisticated Multisim software (Make: National Instrument; Version 11.0) and experimental of the proposed MTJ model based universal logic gates. For both the experimental and simulation studies, we have taken opamp (OP07), $V_1 = V_2 = \pm 4.7V$ and $V_{ref} = +1.000V (-1.000V)$ for NAND (NOR) gate, $R = 4.603k\Omega$, $R_P = 0.567k\Omega$, $R_{AP} = 1.467k\Omega$ and $R_L = 0.977k\Omega$. The experimental, simulated and theoretical results have tabulated in the Table 1 and Table 2 for 2-input NAND and NOR gate. Table 3 shows the corresponding logical current inputs and voltage outputs assuming for input currents, $-1.021mA = \text{logic '0}$ and $+1.021mA = \text{logic '1}$ and for output voltages, negative voltage = logic ‘0 and positive voltage = logic ‘1’. This is obvious from the Tables that the experimental results agree with the simulated and theoretical results and satisfy the truth table [7] of the conventional universal logic gates.

Table 1: Experimental, Simulation and Theoretical results for 2-input NAND logic gate

<table>
<thead>
<tr>
<th>Input currents (mA)</th>
<th>Output voltage ($V_O$) (Volts)</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>Experimental</td>
</tr>
<tr>
<td>$I_1$</td>
<td>$I_2$</td>
</tr>
<tr>
<td>-1.021</td>
<td>-1.021</td>
</tr>
<tr>
<td>-1.021</td>
<td>+1.021</td>
</tr>
<tr>
<td>+1.021</td>
<td>-1.021</td>
</tr>
<tr>
<td>+1.021</td>
<td>+1.021</td>
</tr>
</tbody>
</table>

Table 2: Experimental, Simulation and Theoretical results for 2-input NOR logic gate

<table>
<thead>
<tr>
<th>Input currents (mA)</th>
<th>Output voltage ($V_O$) (Volts)</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>Experimental</td>
</tr>
<tr>
<td>$I_1$</td>
<td>$I_2$</td>
</tr>
<tr>
<td>-1.021</td>
<td>-1.021</td>
</tr>
<tr>
<td>-1.021</td>
<td>+1.021</td>
</tr>
<tr>
<td>+1.021</td>
<td>-1.021</td>
</tr>
<tr>
<td>+1.021</td>
<td>+1.021</td>
</tr>
</tbody>
</table>

Table 3: Logical Current Inputs and Voltage Outputs for 2 input NAND and NOR gates using Table 1 and Table 2

For input currents, $-1.021mA = \text{logic '0}$ and $+1.021mA = \text{logic '1}$

For output voltages, (-) ve voltage = logic ‘0’ and (+) ve voltage = logic ‘1’
CONCLUSION
This research paper focuses mainly on the study and realization of MTJ model based NAND and NOR logic gates and their truth table verifications. The experimental results show excellent agreement with the simulated and theoretical results. The study also fulfill the truth table of the conventional universal NAND and NOR logic gates.

Joyanto Roychoudhary (Department of Electronics and Communication Engineering, Neotia Institute of Technology Management and Science, West Bengal, India)

Sumitesh Majumder (Department of Applied Electronics and Instrumentation Engineering, Netaji Subhash Engineering College, Techno City, Garia, Kolkata – 700 152, West Bengal, India)

T K Maiti (Professor and Head of the department of Applied Electronics and Instrumentation Engineering, Netaji Subhash Engineering College, Techno City, Garia, Kolkata – 700 152, West Bengal, India)

REFERENCES


